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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,506	09/13/2000	Robert Warren Schmidt	RCA 89,970	7961

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/661,506	SCHMIDT, ROBERT WARREN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 06/14/2002. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Crandall (USP 3919655).

For claims 1, 5 and 7 the term "center tapped ground of the spit level power supply" given the broadest reasonable interpretation based on the specification and claims, is interpreted as ground which is center level between the two split of a split level power supply.

For claim 1, Crandall discloses in figure 1 a circuit for operating an amplifier designed for operation with a single ended power supply (the opamp 741 used with split level supply (V+ and V-) is also designed for a single power supply in that it cab also operate to provide an output with only a single supply V+ and ground if such voltages were applied), the circuit comprising: first voltage level translating means (20) for connecting a first polarity power supply terminal of the operational amplifier integrated circuit (741) to a first polarity of the power supply (V+); second voltage level translating means (21) for connecting a second polarity power supply terminal of the operational amplifier integrated circuit to a second polarity of the split level power supply (V-); and means (resistor connected to positive terminal of 741) for connecting a

signal input terminal (positive input terminal of 741) of the operational amplifier to a center tapped ground (ground is the median point between two same voltages with opposite polarity, V+ and V-); and wherein another signal input terminal (inverting input terminal of 741) of the operational amplifier 741 is coupled to a signal source referenced to ground without any DC isolation capacitors connected in series with the amplifier and the output terminal of the operational amplifier is coupled to a signal load referenced to ground without any DC isolation capacitors connected in series with the amplifier.

As to claim 3, Crandall's figure 1 is capable of driving loudspeaker. Therefore, it is seen as an intended use for using Crandall's amplifier circuit to drive the loudspeaker.

For claim 4, it is inherent that the amplifier circuit 741includes a plurality of amplifiers (the amplifier circuit having at least two elements, i.e. transistors. Any circuit elements can be seen as amplifier circuit) integrated on a common substrate having a same substrate bias.

For claim 5, the split power supply (V+ and V-) also provides power to other circuits (16, 17).

As to claim 6, Crandall's power supply is capable of providing power for DVD player, and the circuit figure 1 is capable of driving earphone. Therefore, it is seen as an intended use for using the Crandall's supply voltage as a power signal for the DVD player, and using the amplifier circuit for driving the earphone.

For claim 7, it is inherent that the amplifier has an AC reference input 11 which is connected to the DC ground through the resistor coupled to the positive input terminal of the amplifier.

3. Claims 1, 4, 5, and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Gonda (USP 3818361).

For claim 1, Gonda discloses in figure 5 a circuit for operating an amplifier designed for operation with a single ended power supply (the OP5 used with split level supply (+40 and -40) is also designed for a single power supply in that it cab also operate to provide an output with only a single supply +40 and ground if such voltages were applied), the circuit comprising: first voltage level translating means (the upper Zener diode) for connecting a first polarity power supply terminal of the operational amplifier integrated circuit (OP5) to a first polarity of the power supply (+40); second voltage level translating means (the lower Zener diode) for connecting a second polarity power supply terminal of the operational amplifier integrated circuit to a second polarity of the split level power supply (-40); and means (1KΩ resistor) for connecting a signal input terminal (positive input terminal of OP5) of the operational amplifier to a center tapped ground (ground is the median point between two same voltages with opposite polarity, V+ and V-); and wherein another signal input terminal (inverting input terminal of OP5) of the operational amplifier OP5 is coupled to a signal source referenced to ground without any DC isolation capacitors connected in series with the amplifier and the output terminal of the operational amplifier is coupled to a signal load referenced to ground without any DC isolation capacitors connected in series with the amplifier.

For claim 4, it is inherent that the amplifier circuit OP5 includes a plurality of amplifiers (the amplifier circuit having at least two elements, i.e. transistors. Any circuit elements can be seen as amplifier circuit) integrated on a common substrate having a same substrate bias.

For claim 5, the split power supply (+40 and -40) also provides power to other circuits (the transistor).

For claim 7, it is inherent that the amplifier has an AC reference input Vi which is connected to the DC ground through the resistor coupled to the positive input terminal of the amplifier.

As to claims 8-10, figure 8, figure 5 shows the operational amplifier has a predetermined maximum voltage rating and the split level power supply having a voltage greater than the maximum voltage rating; and the first voltage level translating means and the second voltage level translation means each comprising Zener diode having respective Zener voltages selected to enable the integrated circuit to operate within the maximum voltage rating when powered by the split level power supply.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
March 28, 2003

Terry D. Cunningham
Primary Examiner